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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	R	ATTORNEY DOCKET NO.
08/839,558	04/14/97	ARIMILLI		

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LANE EXAMINER

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ART UNIT	PAPER NUMBER
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4
10/28/98

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action SummaryApplication No.
08/839,558

Applicant(s)

Arimilli

Examiner

D. Langjahr

Group Art Unit

2752 Responsive to communication(s) filed on 4-14-97 This action is FINAL. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire _____ month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims Claim(s) 1-19 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

 Claim(s) _____ is/are allowed. Claim(s) 1-19 is/are rejected. Claim(s) _____ is/are objected to. Claims _____ are subject to restriction or election requirement.**Application Papers** See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948. The drawing(s) filed on _____ is/are objected to by the Examiner. The proposed drawing correction, filed on _____ is approved disapproved. The specification is objected to by the Examiner. The oath or declaration is objected to by the Examiner.**Priority under 35 U.S.C. § 119** Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d). All Some* None of the CERTIFIED copies of the priority documents have been received. received in Application No. (Series Code/Serial Number) _____. received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

 Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).**Attachment(s)** Notice of References Cited, PTO-892 Information Disclosure Statement(s), PTO-1449, Paper No(s). _____ Interview Summary, PTO-413 Notice of Draftsperson's Patent Drawing Review, PTO-948 Notice of Informal Patent Application, PTO-152**— SEE OFFICE ACTION ON THE FOLLOWING PAGES —**

DETAILED ACTION

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claim(s) is/are directed; the following title is suggested: --Dual associative-cache directories allowing simultaneous read operation using two buses with multiplexors, address tags, memory block control signals, single clock cycle operation and error correction.-- or something similar.
3. Claim(s) 1-19 is/are presented for examination.

Claim Rejections - 35 USC § 112

4. Claim(s) 16 and 19 is/are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim(s) 16 recite(s) the limitation "...said address tags..." in line(s) 4, 8 and 13. There is insufficient antecedent basis/bases for this/these limitation(s) in the claim(s).

Appropriate correction is required for all paragraphs above. In the rejections below please note that (for example) C 1, L 6 refers to column 1, line 6 of the prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

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A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. This application currently names joint inventors. In considering patentability of the claim(s) under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

6. Claim(s) 1-19 is/are rejected under 35 U.S.C. 103 as being unpatentable over Kalish in view of Lee.

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Kalish et al., U.S. Patent 5553263 discloses the claim limitations shown above, including {claim(s) 1 , 10, 11} accessing cache values, loading the cache from memory, writing address tags associated with memory blocks is expressed or implied in the abstract, reading first and second memory blocks at the same time taught as...simultaneous processor requests and internal invalidation operations can be simultaneously performed independently in the respective operational sections (C 4, L 56), {claim(s) 9, 19} error correction taught as...the cache memory system could be rendered fault tolerant by utilizing a back-up redundant off-line cache memory system. (C 3, L 4), {claim(s) 3, 4, 14, 15} multiplexor taught as...The invalidation queue 71 and the block address counter logic 73 provide an invalidation address input 75 to an address multiplexer 76. (C 9, L 18), {claim(s) 6, 16} congruence classes taught as...the number of directory sets into which address requests can be mapped has diminished, i.e., the set associativity of the degraded cache has been reduced (C 3, L 41), {claim(s) 7, 8, 17, 18} first (second) bus connected to first (second) multiplexor taught as...the multiplexer 76 via buses 95 and 96 (C 10, L 61).

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However, Kalish does not particularly and explicitly disclose first and second cache directories, control signal for memory blocks, read in a single clock cycle, comparison, bus on the processor side and another on the system side.

Searching the references for the relevant analogous concepts of redundant directories and buses, block control signals, single-cycle access, the closest analogous art seems to be Lee et al., U.S. Patent 5345576; he is found to solve generally similar problems. These issues are directly relevant to the claim(s) listed above.

Lee discloses {claim 1, 2, 10, 11, 13} a) first and second cache directories (Fig. 1 items 12 and 22), {claim(s) 3, 4, 14, 15} b) control signal for memory blocks taught as...BNewBlk# Backside Bus New Block indication. This is asserted during the first cycle of an access. This is used to synchronize with the external logic. BNewBlk# is asserted low. (C 6, L 11), {Claim(s) 5, 12} c) first and second blocks are read in a single clock cycle implied as ...The cache is comprised of a data RAM (16) which is an array of synchronous SRAM that operates at 32 MHZ. It is capable of providing 64 bits of data to the processor every clock cycle (C 5, L 3)

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{Claim(s) 6, 16} d) comparison (abstract) for the desirable purpose of a) advantageous for searches (disclosed in "Background Art"); b) necessary for data coherency and speed; c) desirable for speed and minimum design complexity; d) comparison being necessary for system architectural functioning.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to add the features of Lee to the work of Kalish because the reasons stated above was/were known at that time to be reasonably pertinent to the art of Kalish for the desirable purpose disclosed above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

USPN 5,283,876 [Tague] teaches a virtual memory unit with a plurality of directory and buffer store levels for storing page descriptor information. The memory directories and a least recently used (LRU) device constructed from the same type of standard cache address directory part include parity error detection circuits.

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8. Any response to this action should be mailed to:

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or faxed to:

(703) 308-9051 (for formal communications intended for entry)

Or:

**(703) 308-6606 (for informal or draft communications, please label
"PROPOSED" or "DRAFT");**

**Hand-delivered responses should be brought to Crystal Park II, 2121
Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).**

**9. Any inquiry concerning this communication or earlier communications from
the examiner should be directed to David Langjahr whose telephone number is
(703) 305-4034 (e-mail address: David.Langjahr@uspto.gov). The examiner can
normally be reached Monday through Thursday from 7:00 AM to 5:30 PM. If
attempts to reach the examiner by telephone are unsuccessful, the examiner's
supervisor, Tod Swann, can be reached on (703) 308-7791.**

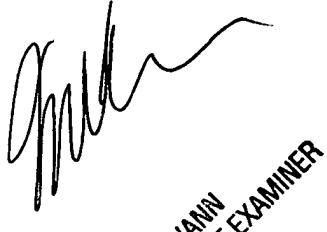
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The fax phone number for this Group is (703) 308-6606. It is recommended that any faxes sent be followed by a voicemail message to (703) 305-4034 stating that a fax has been sent, and by whom. Also, please include a return phone number.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

DCL

DCL
October 7, 1998



TOD R. SWANN
SUPERVISORY PATENT EXAMINER
GROUP 2700